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# Design and Implementation of DDR3 Controller with AXI Compliancy

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**Abstract:** This project describes Design and Implementation of DDR3 Controller with AXI Compliancy. It explains the architecture of the DDR3 controller along with the detailed design and operation of its individual sub blocks. It also discusses the advantage of DDR3 memories over DDR2 memories and the AXI protocol operation. The AXI DDR3 Controller provides access to DDR3 memory. It accepts the Read / Write commands from AXI and converts it into DDR3 access. While doing this it combines AXI burst transactions into single DDR access where ever possible to achieve the best possible performance from DDR3 memory subsystem.

**Keywords**: Verilog HDL, Xilinx ISE, Model Sim Simulator, AXI, DDR3 Memory, DDR3 Controller, FIFO.

## I. INTRODUCTION

A bus protocol that supports separate address/control and data phases, unaligned data transfers using byte strobes, burst-based transactions with only start address issued, separate read and write data channels to enable low-cost DMA, ability to issue multiple outstanding addresses, out-of-order transaction completion, and easy addition of register stages to provide timing closure. The AXI protocol also includes optional extensions to cover signalling for low-power operation. AXI is targeted at high performance high clock frequency system designs and includes a number of features that make it very suitable for high speed sub-micron interconnects.

The Memory is being improved to achieve high speed, low power consumption, cost-effective. DDR3 proves to achieve such goal. AXI compliant DDR3 Controller permits access of DDR3 memory through AXI Bus interface. The DDR3 controller works as an essential bridge between the AXI host processor and DDR3 memory. It takes care of the DDR3 initialization and various timing requirements of the DDR3 memory. The DDR3 controller uses bank management modules to monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. In order to enhance overall performance, SDRAMs offer features including multiple internal banks, burst mode access, and pipelining of operation executions. Accessing one bank while precharging or refreshing other banks is enabled by the feature of multiple internal banks. By using burst mode access in a memory row, current SDRAM architectures can reduce the overhead due to access latency. The pipelining feature permits the controller to send commands to other banks while data is delivered to or from the currently active bank, so that idle time during access latency can be eliminated.

The work carried out is described in brief as follows; Section II explains the Literature Survey, Section III represents the AXI Protocol Specification. Section IV describes the Implementation of DDR3 controller with AXI Compliancy. Section V shows Simulation Results and Discussions of the Project**,** Section VI concludes this paper.

## II.LITERATURE SURVEY

Shrinking process technologies and increasing design sizes have led to highly complex billion-transistor integrated circuits (ICs). As a consequence, manufacturers are integrating increasing numbers of components on a chip. A heterogeneous system-on-a-chip (SoC) might include one or more programmable components such as general purpose processors cores, digital signal processor cores, or application specific intellectual property (IP) cores, as well as an analog front end, on-chip memory, I/O devices, and other application specific circuits.

**AMBA:** AMBA, is a bus standard devised by ARM with aim to support efficient on-chip communications among ARM processor cores. Nowadays, AMBA is one of the leading on-chip busing systems used in high performance SoC design. AMBA is hierarchically organized into two bus segments, system- and peripheral-bus, mutually connected via bridge that buffers data operations between them. Standard bus protocols for connecting on-chip components generalized for different SoC structures, independent of the processor type, are defined by AMBA specifications.

**Double Data Rate:** DDR memory controllers are used to drive DDR SDRAM, where data is transferred on the rising and falling access of the memory clock of the system. DDR memory controllers are significantly more complicated than Single Data Rate controllers, but allow for twice the data to be transferred without increasing the clock rate or increasing the bus width to the memory cell. Data transfer comparison between SDRAM and DDR SDRAM is shown in figure1.

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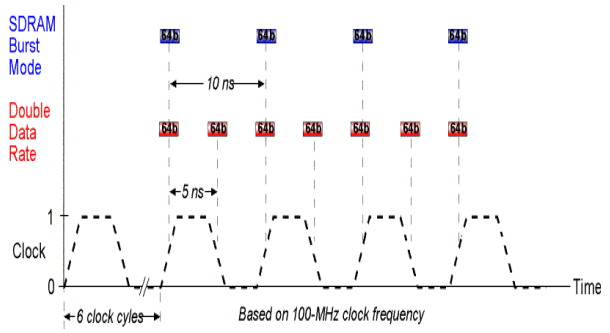


Figure1. Data transfer rate comparison between SDRAM and DDR SDRAM

## III.AXI PROTOCOL SPECIFICATION

The AMBA AXI protocol is targeted at high-performance, high-frequency system designs and includes a number of features that make it suitable for a high-speed submicron interconnects.

The AXI protocol is burst-based. Every transaction has addressed and control information on the address channel that describes the nature of the data to be transferred. The data is transferred between master and slave using a write data channel to the slave or a read data channel to the master. In write transactions, in which all the data flows from the master to the slave, the AXI protocol has an additional write response channel to allow the slave to signal to the master the completion of the write transaction.

The AXI protocol enables out-of-order transaction completion. It gives an ID tag to every transaction across the interface. The protocol requires that transactions with the same ID tag are completed in order, but transactions with different ID tags can be completed out of order. Out-of-order transactions can improve system performance.
The AXI protocol defines three burst types:

- Fixed burst.
- Incrementing burst.
- Wrapping burst.

**Fixed burst:**

In a fixed burst, the address remains the same for every transfer in the burst. This burst type is for repeated accesses to the same location such as when loading or emptying a peripheral FIFO.

**Incrementing burst:**

In an incrementing burst, the address for each transfer in the burst is an increment of the previous transfer address. The increment value depends on the size of the transfer.

**Wrapping burst:**

A wrapping burst is similar to an incrementing burst, in that the address for each transfer in the burst is an increment of the previous transfer address. However, in a wrapping burst the address wraps around to a lower address when a wrap boundary is reached.

## IV. IMPLEMENTATION OF DDR3 CONTROLLER WITH AXI COMPLIANCY

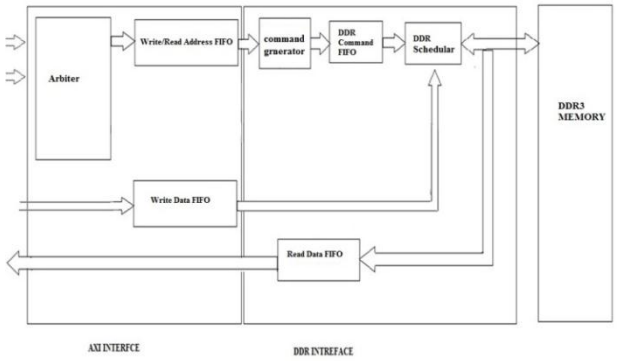


Figure2. Block Diagram of AXI compliant DDR3 controller

The design consists of following blocks.

- AXI interface
- DDR interface

The AXI DDR3 Controller provides access to DDR3 memory. It accepts the Read / Write commands from AXI and Converts it into DDR3 access. While doing this it combines AXI burst transactions into single DDR access where ever Possible to achieve the best possible performance from DDR3 memory subsystem. DDR3 memory interacts with the DDR3 interface and AXI channels are interact with the AXI interface.

**Block diagram Description:**

The arbiter block is selecting the one request either read request or write request when two requests are valid. The selection of request based on the previously completed write or read request. After select the R/W request, the request stored in the write/ read address channel FIFO. These signals are stored in the FIFO memory location, from wrt_ptr and based on the space available in the FIFO memory location each request is stored in FIFO one location.

The main purpose of the command generator is to generate the command for the memory. Depending on address lines command generator performs the operation. The inputs of the command generator taken from output of Write/Read address channel FIFO rd_ptr. Based on the given address the command generator generate the required commands (active, precharge, LMR, write, read) for the DDR3 memory

The Command scheduler will take the commands from the command FIFO and generate the required signals (RASb, CASb, WEb) for the DDR memory. The command scheduler will not process all the commands at the same time.

The DDR memory can store the write data into memory and by using the memory signals (RASb, CASb, WEb, CSb, CKE, RESET, CK, DQ, DQM).

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**Simplified State Diagram of the DDR Scheduler**

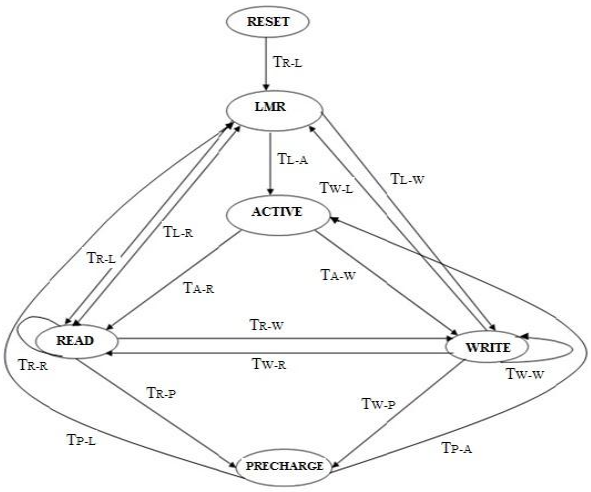


Figure3. Simplified State Diagram of the DDR Scheduler

## V.SIMULATION RESULTS

The Simulation Results are observed in Model sim Simulator and Synthesis Reports are taken from Xilinx ISE simulator. The Timing Descriptions are taken from Xilinx tool.

**Simulation results for AXI compliant DDR3 memory**

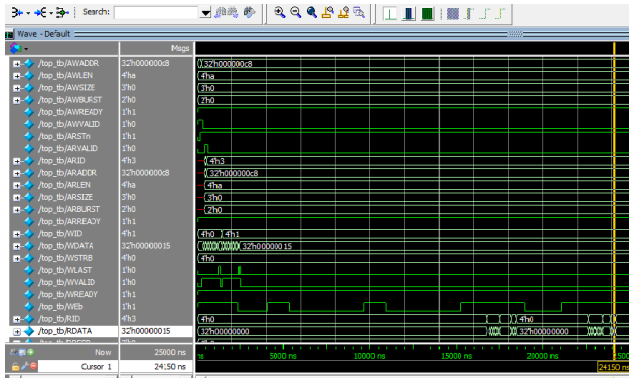

Figure4. AXI compliant DDR3 memory

**Description:**

In the above Simulation Results, I sent the eight 32 bit Transactions (Fixed Burst Type) from Write Data Channel to the 32 bit Address location from Write Address Channel and Retrieved the same eight 32 bit Transactions from Read Data channel from the 32 bit Address location from Read Address Channel.

The AXI Channels works with Handshake Signals (VALID, READY). The transaction should start when VALID and READY signals are high and it depends on the type of handshake mechanism that we taken like VALID before READY, VALID after READY, VALID equal to READY. The WLAST signal is used to indicate the end of the last Transaction with ID specified for each burst type.

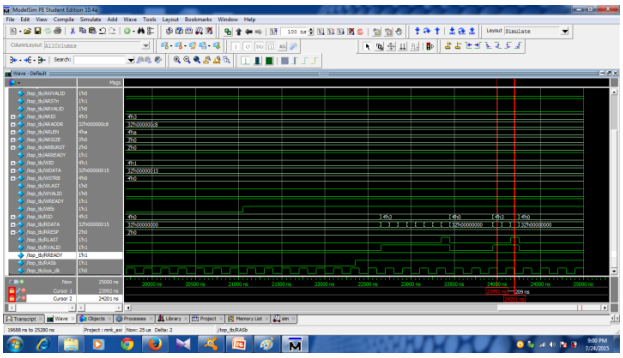

Figure5. Observation of Clock with Respect to DDR

**Description:**

As DDR Stands for Double Data Rate, the transferring of data is done on both Rising and Falling edges of clock signal.

**RTL Schematic for AXI compliant DDR3 memory**

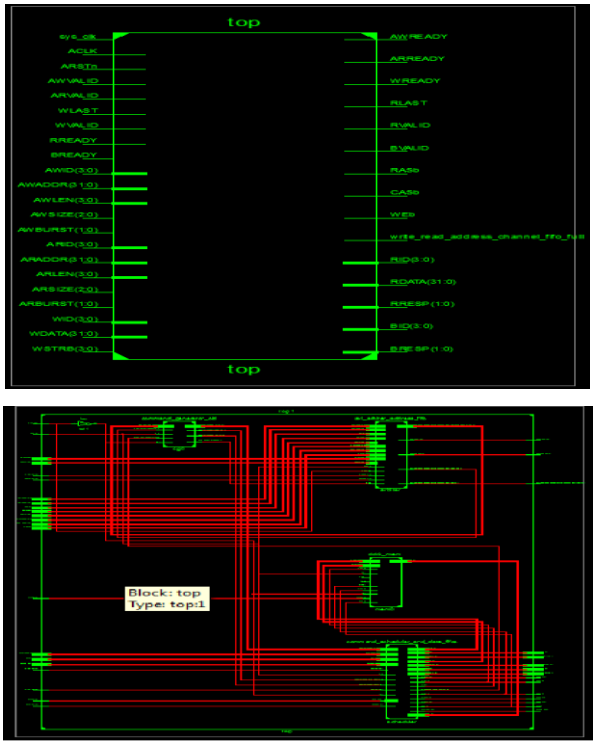


Figure6. RTL Schematic for AXI compliant DDR3 memory

**Description:**

If we observe the above schematic, The Handshake signals VALID and READY are given to Arbiter and the Arbiter will send corresponding Read and Write signals to Arbiter FIFO. The Command Generator will generate the commands based on requests coming taken from Arbiter FIFO.

The Generated commands are given to Scheduler; The Scheduler will provide the priority based on requests coming from Write Data Channel and Read Data Channel. The DDR3 Memory works based on the scheduler commands weather to Read Data from Memory to Read Data Channel or Write Data to Memory from Write Data Channel.

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**Timing Report**

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Minimum period                    : 5.364ns
(Maximum Frequency: 186.444MHz)
Minimum input arrival time before clock   : 2.822ns
Maximum output required time after clock  : 1.920ns
Maximum combinational path delay          : 1.206ns

Total REAL time to Xst completion         : 344.0 secs
Total CPU time to Xst completion          : 343.5 secs

Total memory usage is 399564 kilobytes
=================================
```

## VI.CONCLUSION

The transactions are transferred repeatedly, without any delay in between, and its maximum operation frequency is 186.4 MHz we performed the AXI interface with respect to one master and one slave. This design supports AXI protocol (32 or 64 bit) data width, remapping, run time configurable timing parameters & memory setting, delayed writes, multiple outstanding transactions and also supports the automatic generation refresh sequences. We examined the performance of the design by generating different type of commands and noting down the time taken by the DDR3 controller in finishing them, as the path delay between scheduler to write_data_channel_fifo is 5.364ns and the path delay between arbiter to write_read_address_channel_fifo is 1.920ns.The latency of the design is between 10 to 35 clocks based on the command generated and the internal DDR state.

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